ONLINE
SHORT TERM TRAINING PROGRAMM
On
RECENT TRENDS IN ELECTRONIC COMMUNICATION AND SEMICONDUCTORS Workshop

On 10th June 2024 to 14th June 2024

Organized By

Akhil Bharatiya Maratha Shikshan Parishad's

Anantrao Pawar College of Engineering & Research, Parvati, Pune - 411 009

In Association With

Indian Society for Technical Education

About the Institute: Anantrao Pawar College of Engineering and Research is situated in nation's education hub, Pune and recognized for its quality education and research. The institute is established in 2012 having 8 UG, 4 PG & 6 B.Voc courses affiliated to Savitribai Phule Pune University. Institute is committed to impart quality technical education as per the needs & acceptation of all the stakeholders. APCOER, Pune is under the mentorship of College of Engineering Pune (COEP). National & Internationally recognized research are involved in the Innovation club of Institute guiding the faculties & students for product development, startups & to become entrepreneur through business incubation center. APCOER, Pune is committed to comprehensive development of students through quality technical education.

Institute Vision: Committed to comprehensive development of students through quality technical education.

Institute Mission: 1) To Provide state of art infrastructure that shallcreate ambience to encourage novel ideas, research activities and consultancy services.

2) To inspire students in creation & entrepreneurship. 3) To create future technocrats with intelligence, technical skills & good ethical moral values so as to serve needs of society & industries.

4) To provide healthy Teaching-Learning environment that will cultivate contemporary research activities, innovations & inventions.

5) To develop center of excellence in technical education.

Day wise Schedule & Keynote Speaker

Day 1: 10/06/2024 Time 10:00-01:00 PM
Session 1: Inauguration and Session on VLSI Design by Dr. Vijay Wadhai
President, cyber security corporation Pune

Day 1: 10/06/2024 Time 02:00-05:00PM
Session 2: Challenges in Designing 5G high speed CMOS Digital Systems by Dr. Shaila Subbaraman, Ex. Dean Academics of Autonomous Walchand College of Engineering, Sangali

Day 2: 11/06/2024 Time 10:00-01:00 PM
Session 1: Semiconductor Technologies by Dr. Vaishali Ingale, Associate Professor, COEP, Pune

Day 2: 11/06/2024 Time 02:00-05:00 PM
Session 2: Semiconductor Manufacturing Techniques by Dr. Vaneeta Agarwal, Assistant Professor, COEP, Pune

Day 3: 12/06/2024 Time 10:00-01:00 PM and 02:00-05:00 PM
Session 1& 2: Microwave Communication by Dr. S. V. Gaikwad,
Associate Professor, PICT , Pune

Day 4: 13/06/2024 Time 10:00-01:00 PM
Session 1: CMOS Technology Dr. Seema Rajput, Associate Prof, Cummins College of Engi. Pune

Day 4: 13/06/2024 Time 02:00-05:00 PM
Session 2: 5 G Technology by Dr. Prachi Mukherji, Professor, Cummins College of Engi. Pune

Day 5: 14/06/2024 Time 10:00-01:00 PM
Session 1: Design of CMOS Analog Circuit by Dr. Ashok Saraf, Trustee Science & Technology Park, S. P. Pune University

Day 5: 14/06/2024 Time 02:00-05:00 PM
Session 2: IP Implementation FPGA Technology Experience Sharing by Er. Sudarshan Natu, Managing Director, Nital Computer Systems Pvt. Ltd.Pune

Registration Form

Name: .....

Designation:.....

Name of Institute: .....

Mobile No:.....

Email Id:.....

Member of ISTE: Yes/No

ISTE Membership Number:.....

Applicant's Sign

HOD / Principal Sign

Registration Link:

https://forms.gle/R8JknKrkVERXNtFg8

Registration Fees:
Rs. 250/-

Note: Participants will receive certificates only after attending all the sessions and scoring 60% in the test. Feedback form willbe circulated at the end of each session of STTP.

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About STTP:

Designing a comprehensive training program for faculty in Electronics Communication, Semiconductor Technologies, and 5G involves several key components. The program should be structured to enhance the technical knowledge, pedagogical skills, and research capabilities of the faculty members.

Organizing Committee

Prof. Snehal Veer
Prof. Vaishali Bhimte
Prof. Sharad Jagtap
Prof. Swati Gandhi
Prof. Kishor Jadhav
Prof. Ashwini Suryawanshi
Prof. Prachi Upasani
Prof. Nikita Bhagat

E & TC Department Vision:

To strive students for affirming quality through innovation in technical education.

E & TC Department Mission:

1. To contribute in magnified education that enumerates and accomplishes brilliance in teaching learning process and innovation.
2. To create passion amongst students for contributing to research by providing industry exposure.
3. To inspire students and faculty by providing them various opportunities with industry oriented learning
4. To develop professional attitude, moral and ethical values among students for society.

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Principal, Anantrao Pawar College of Engineering & Research.

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IQAC Co-ordinator

Prof. G. E. Kondhalkar
Mechanical Engineering Department

STTP Co-ordinator

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Mr. S. V. Natu
Managing Director Nital Computer System Pvt. Ltd., Pune

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CEO, JyoSH Al Soluions Pvt. Ltd.

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	Report On STTP Attended By Faculty	

ONE WEEK ONLINE SHORT TERM TRAINING PROGRAM ON RECENT TRENDS IN ELECTRONIC COMMUNICATION AND SEMICONDUCTORS IN ASSCOCIATION WITH INDIAN SOCIETY FOR TECHNICAL EDUCATION (ISTE)

Name of Event: STTP on "Recent Trends in Electronic Communication and Semiconductors"

Date of Event: 10th June 2024to 14th June 2024

Organized By: ABMSP' APCOER Department of Electronics and Telecommunication Engineering in association with Indian Society for Technical Education (ISTE)

Time of event: 10.00 AM to 5:00 PM

Name of Event Coordinators: Prof. Ashwini Suryawanshi

Number of Participants: 105

Short term training program objective:

Designing a comprehensive training program for faculty in Electronics Communication, Semiconductor Technologies, and 5G involves several key components. The program should be structured to enhance the technical knowledge, pedagogical skills, and research capabilities of the faculty members.

Inauguration Session (10 AM to 10.30 AM)

Short term training program started at 10 AM in the presence of and very eminent personalities, Dr. S. B. Thakare (Principal, APCOER), Dr.Vijay Wadhai (President, Cyber Security Corporation Pune), Mrs. Minakshee Patil (Assistant Professor, Sinhgad Academy of Engineering, Pune) Dr. Rashmi Mahajan (Assistant Professor, MIT, Pune) , Dr. Shaila Subrahmanan (Ex. Dean Academics of Autonomous Walchand College of Engineering, Sangali) , Dr. A. B. Deshmukh (HOD, E&TC Dept., APCOER) & all respectives. Program coordinator Prof. Ashwini Suryawanshi gives briefs about Vision, Mission of institutes and department and Short term training program objective. Dr. S. B. Thakare sir addresses the gathering and explains the need and innovation in communication and semiconductor field. At 10.30 AM Prof. Snehal Veer gives introduction speech of all guests and the short term program was started at 10. 30 AM.

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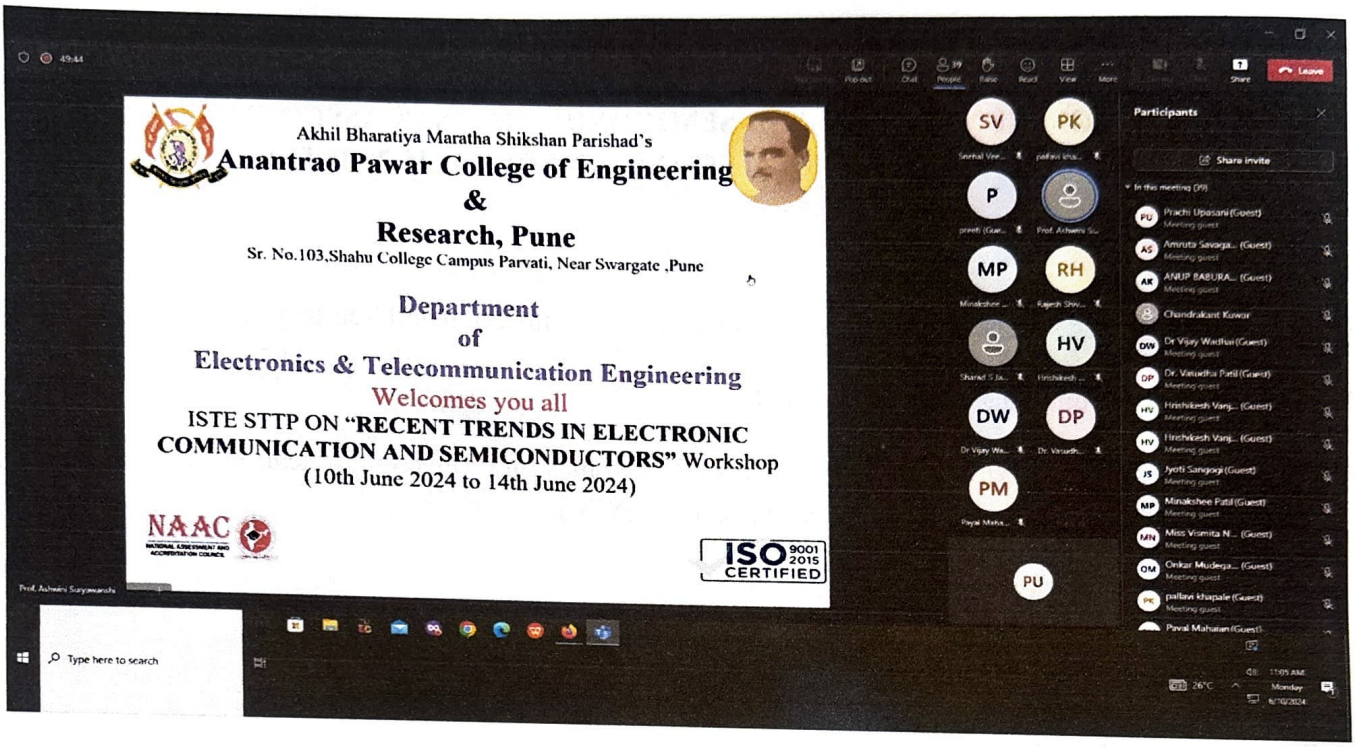
Report On STTP Attended By Faculty



Inauguration Session

Name Of the Day-1 Session Co-ordinator: Prof. S. M. Veer

Day 1 - Session 1 (10.30 AM to 11.30 AM)

Name of resource Person/ Speaker: Dr. Vijay Wadhai (President, Cyber Security Corporation Pune)

Brief Introduction of Resource Person/Speaker:

Dr. Wadhai Sir currently serves as the Principal and Professor at DY Patil College of Engineering, he has held this position since June 2018. His extensive career in academia spans numerous prestigious institutions where he has held significant leadership roles, including Principal and Professor. He has been worked as Principal & Professor at Trinity Academy of Engineering (2 Years), Sinhgad Technical Education Society (3 Years), and MAEER's MITCOE (6 Years) in Kothrud, Pune. He has a rich background in both academic administration and strategic planning, Dr. Wadhai has been instrumental in guiding institutions towards achieving autonomy, accreditation to NBA and NAAC quality standards. Dr. Wadhai's academic expertise is equally impressive. He holds a PhD in Electronics and

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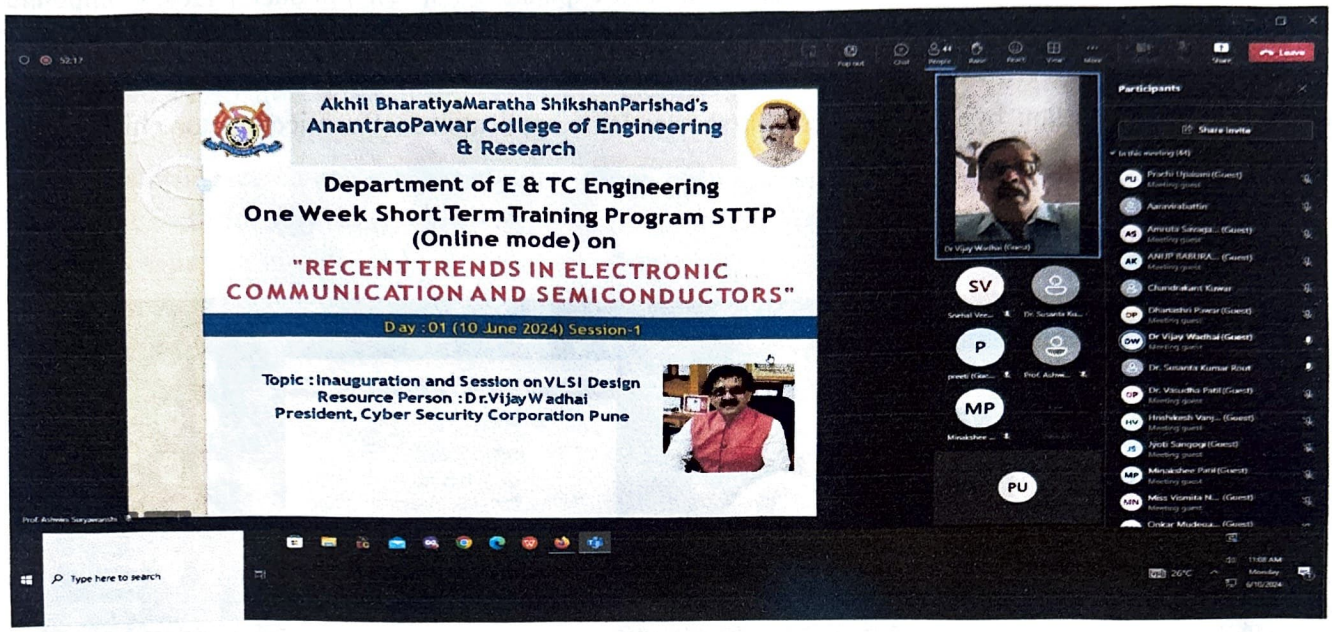
Telecommunication Engineering from Sant Gadge Baba Amravati University and an M.E. in Power Electronics from Gulbarga University. He has authored over 200 research papers, holds 21 patents, and has published 8 books/ chapters. Dr. Wadhai has also successfully guided 16 PhD candidates.



Dr. Vijay Wadhi sir explain about basic of VLSI design

Day 1 - Session 1 (11.30 AM to 12. 30 PM)

Name of resource Person/ Speaker: Prof. Minakshee Patil (Assistant Professor, Sinhgad Academy of Engineering, Pune)

Brief Introduction of Resource Person/Speaker:

Prof. Minakshee Patil has 19 Years of Professional Teaching Experience of UG and PG as Assistant Professor. She is pursuing PhD in Electronics and Telecommunication Engineering from Savitribai Phule Pune University. She has received Research grant of Rs 3, 00,000/- from BCUD (University of Pune). She has Published 1 Patent, 2 books, 3 Book Chapters and 25+ research papers (SCIE, Scopus, and IEEE). Also she has worked as NAAC Co-ordinator in Sinhgad Academy of Engineering, Pune. She has strong analytical, logical and mathematical skills.

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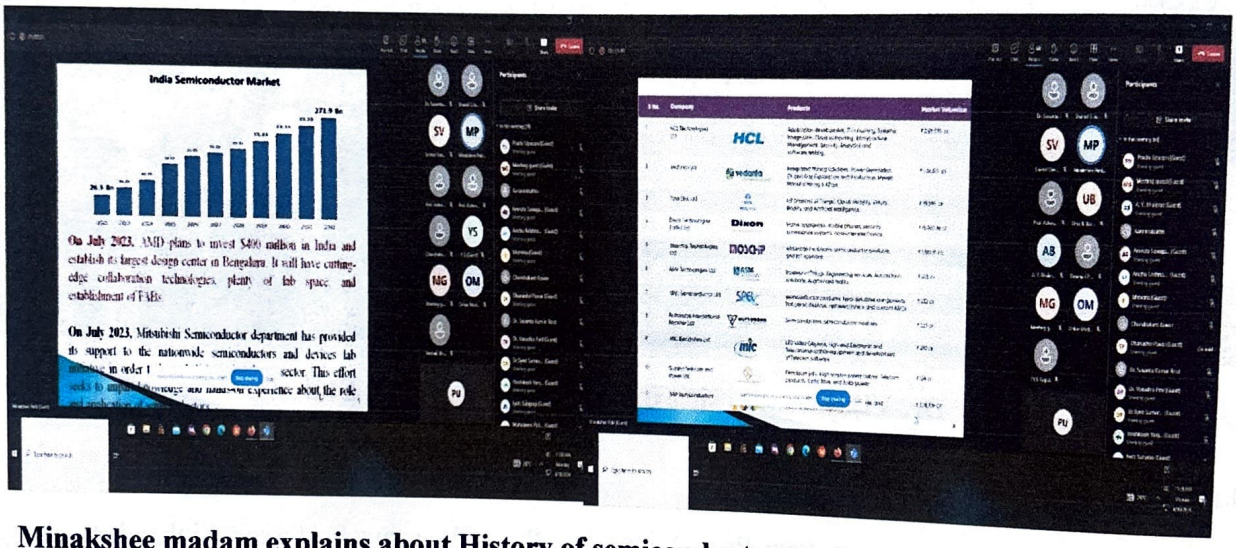
Report On STTP Attended By Faculty

Day 1 - Session 1 discussion –

Prof. Minakshee Patil madam explains about History of semiconductors, its production, current semiconductor production and market scenario, she also explains about semiconductor fabs, Compound semiconductor, Semiconductor design companies and laboratory. The industry's annual semiconductor sale revenue has since grown to over $481 billion, as of 2018 andthe semiconductor industry is projected to reach $726.73 billion by 2027. At the last she explains applications of semiconductor chip and IC fabrication flow.

Photographs of day 1 Session1



Minakshee madam explains about History of semiconductor production and market& current semiconductor production and market scenario

Application of semiconductor Chip & IC fabrication flow explanation

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Day 1 - Session 1 (12. 30 PM TO 1.30 PM)

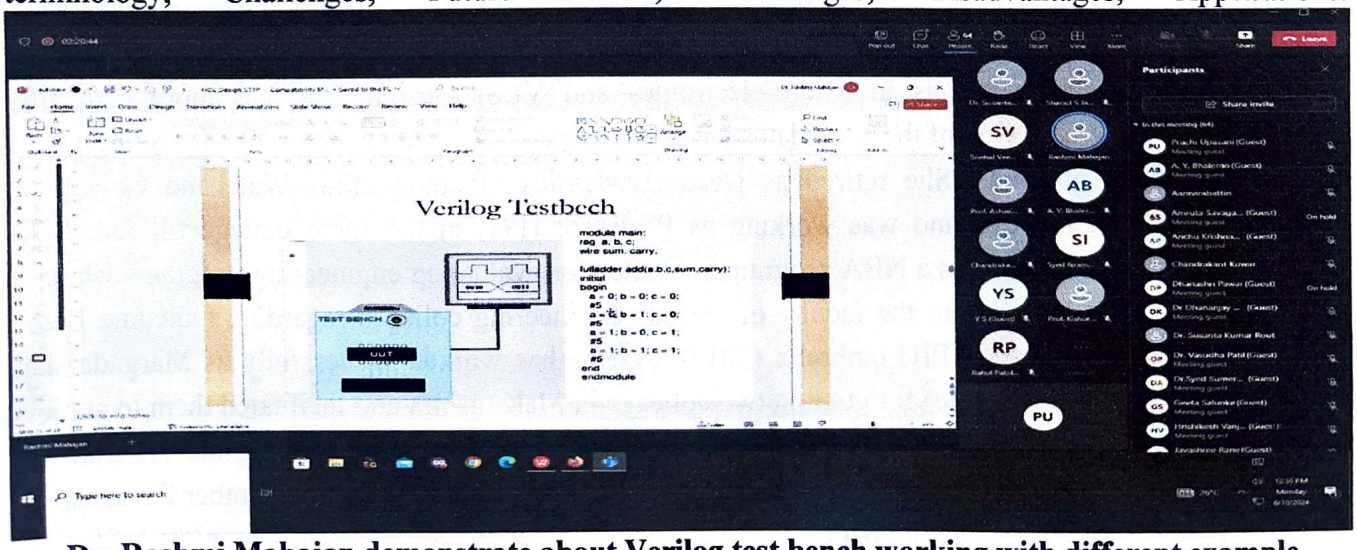
Name of resource Person/ Speaker: Dr. Rashmi Mahajan (Assistant Professor, MIT, Pune)

Brief Introduction of Resource Person/Speaker:

Dr. Rashmi Mahajan is Ph.D. in Electronics Engineering from Kavayitri Bahinabai Chaudhary North Maharashtra University, Jalgaon. She has expertise in VLSI technology and has successfully completed BCUD funded research projects at Savitribai Phule Pune University. Her multi-disciplinary work profile extends in Embedded System, Artificial Intelligence and Machine Learning. She has published more than 22 research papers in various SCI/SCOPUS indexed journals and conferences. In her vast 20 years of service, she has contributed immensely in the field of research, academics as well as administrative work. She has been invited as a Guest and Subject Expert by many reputed Engineering colleges all over Maharashtra. Her work ethics and subject domain expertise has won her many accolades.

Day 1 - Session 1 discussion –

Dr. Rashmi Mahajan madam explains semiconductor chip design flow, VLSI chip Design, VLSI chip classification, details about CPLD, FPGA design, She also explains Verilog testbench with some examples. She said that creating a VLSI chip consists of arranging millions of small transistors on a tiny silicon chip. Two types that exist are ASIC (designed to fulfil particular functions) and FPGA (reprogrammable for different applications). Just like defining the functions of a chip to placing components correctly in multiple verifications of their quality to ensure they operate correctly dictates the process. She also covers VLSI chip classification, working principles, construction and terminology, Challenges, Future Trends, Advantages, Disadvantages, Applications.



Dr. Rashmi Mahajan demonstrate about Verilog test bench working with different example

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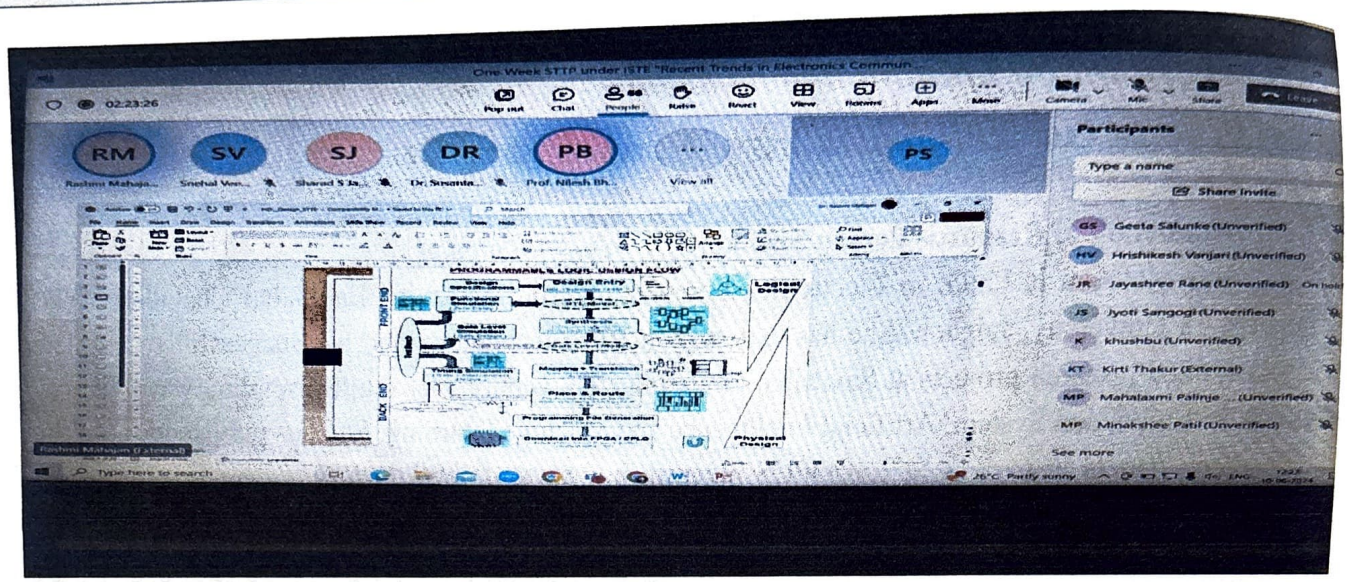

Dr. Rashmi Mahajan explains program logic design flow

Day 1 - Session 2 (2PM TO 5 PM)

Name of resource Person/ Speaker:

Dr. Shaila Subbaraman (Ex. Dean Academics of Autonomous Walchand College of Engineering, Sangali

Brief Introduction of Resource Person/Speaker:

Dr. Shaila Subbaraman, Ph. D. from I.I.T., Bombay (1999) and M. Tech. from I.I.SC., Bangalore (1975) has a vast experience in industry (1975 – 89) in the capacity of R & D engineer and Quality Assurance Manager in the field of manufacturing semiconductor devices and ICs. She also has more than 31 years of teaching experience (1989-2020) at both UG and PG level for the courses in Electronics Engineering. She is a recognized Ph. D guide of Shivaji University, Kolhapur. She has to her credit nine doctorates. Her specialization is in Micro-electronics and VLSI Design. She has more than fifty publications to her credit. One of the candidates has been awarded two patents on the Ph. D work pursued by him under her guidance. She retired as Dean Academics of autonomous Walchand College of Engineering, Sangli in 2010 and was working as Professor (PG) in the same college till Jan 2020. Additionally, she has worked as a NBA program evaluator for evaluating engineering programs while as an expert for giving guidance to the faculty of various engineering colleges regarding Outcome Based Education philosophy under NPIU umbrella (2017-19). She has worked successfully as Margadarshak during 2019-23 (AICTE Scheme) for guiding two colleges in Maharashtra and facilitated them to achieve the NBA accreditation. She also worked as an NBA expert (2013-16) for assessing the programs of various colleges in India. Additionally, she was also involved as AICTE committee member for assessing the educational institutes in Punjab, MP, UP and Himachal Pradesh for extension of approval. She was felicitated in 2017 by "Pillars of Hindustani Society" award instituted by Trans-Asia Chamber of Commerce, Mumbai for her contribution to Higher Education in Western Maharashtra.

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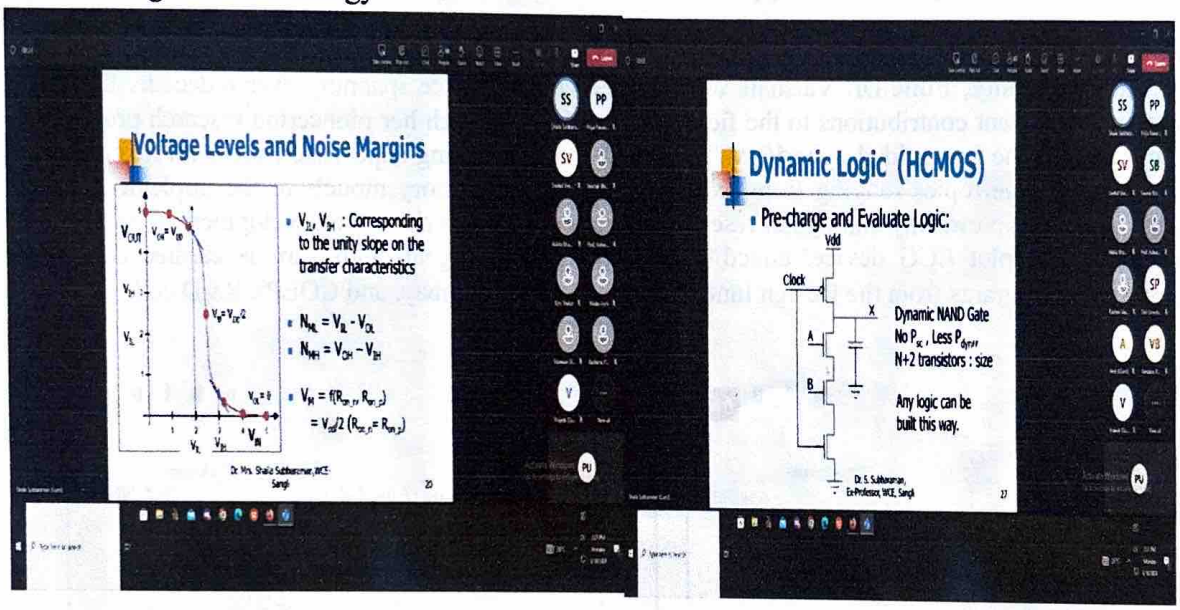
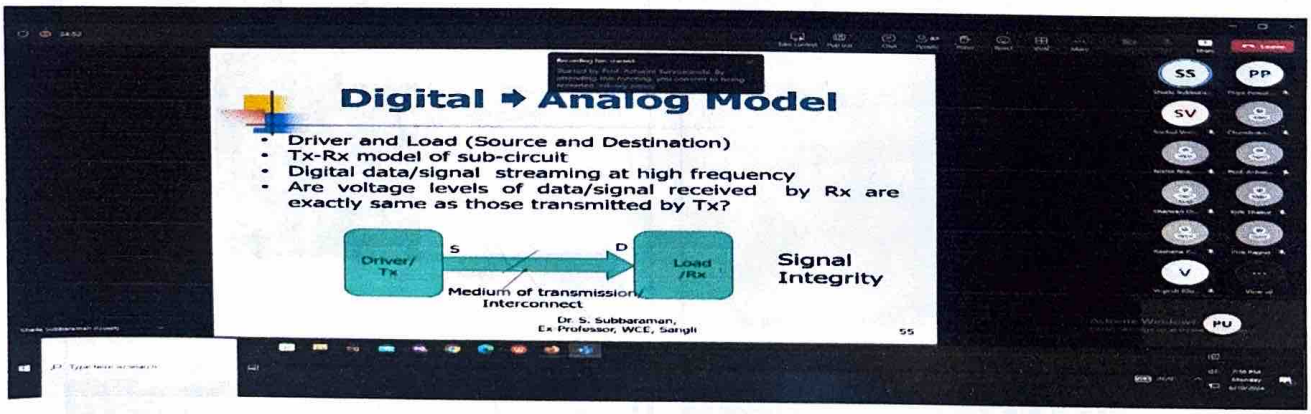
Day 1 - Session 2 discussion –

Dr. Shaila Subbaramanmadam explains about the design of 5G high speed CMOS digital systems, issues and solutions in HSDS design, Different types of crosstalk, Different characteristic voltages and noise margin, 5G requirements, its speed, and its coverage, application of 5G, advantages and challenges, CMOS design and technology.



Dr. Shaila Subbaraman madam explains different characteristics for chip design



Dr. Shaila Subbaraman madam explains digital Analog model

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Report On STTP Attended By Faculty

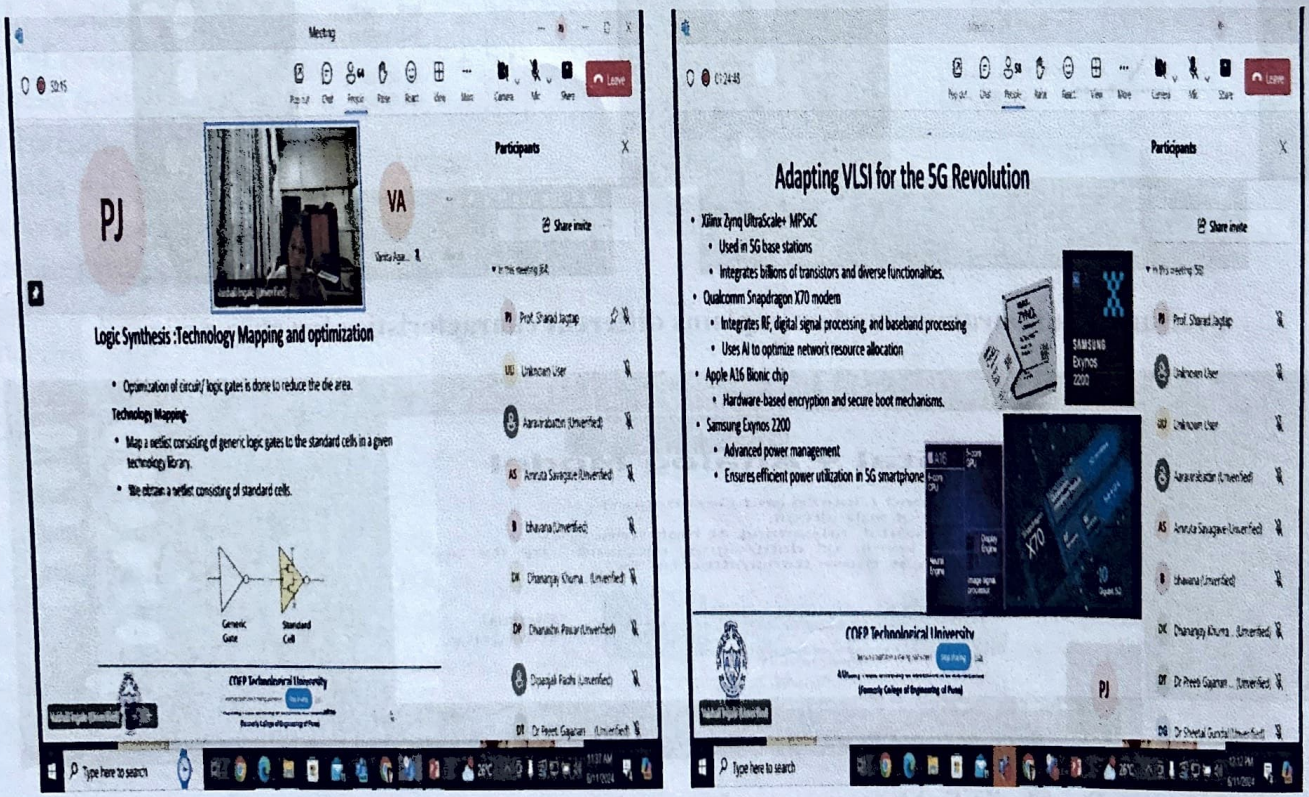
Day 2: 11/06/2024

Name Of the Day-1 Session Co-ordinator: Prof. Sharad Jagtap

Session 1- Semiconductor Technologies (10:00 am – 01:00 pm)

Name of resource Person/ Speaker (If Applicable): Dr. Vaishali Ingale

Brief Introduction of Resource Person/Speaker: Dr. Vaishali Ingale is working as associate professor at COEP Tech. University, Pune.Dr. Vaishali With a research experience spanning over a decade, Dr. Ingale madam has made significant contributions to the field of technology through her pioneering research projects and scholarly publications. She has guided over 50 M.Tech theses, with ongoing supervision for 2 more, covering a wide array of cutting-edge topics ranging from reconfigurable cache memory models to the implementation of secure microprocessors. Noteworthy among her research endeavors is her work on the development of an Android-based 12 Channel Life plot ECG device, aimed at classifying ECG signals into various cardiac conditions, supported by prestigious grants from the Design Innovation Centre, IIT Bombay, and COEP's R&D cell.



Dr. Vaishali Ingale Explaining Logic Synthesis process

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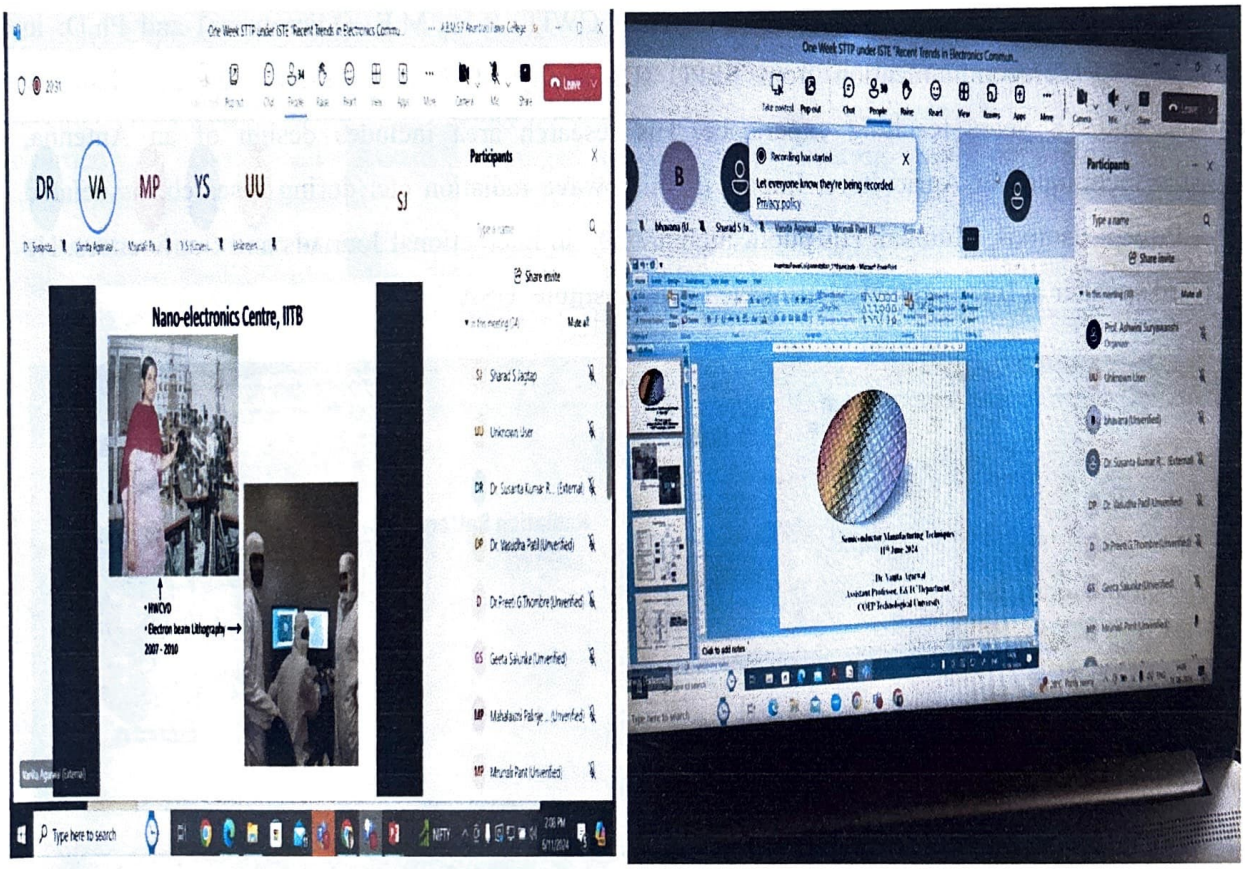
Report On STTP Attended By Faculty

Session 2: Semiconductor Manufacturing Techniques(02:00 pm – 05:00 pm)

Name of resource Person/ Speaker (If Applicable): Dr. Vanita Agarwal

Brief Introduction of Resource Person/Speaker: Dr. Vanita Agarwal is working as Assistant Professor at COEP Tech. University, Pune.Dr. Agarwal's expertise extends beyond academia; she has also actively contributed to the advancement of technology in the industry. As a reviewer for prestigious technical journals like the IEEE IoT Journal (2017 2018) and IEEE Systems Journal (2019), she has played a crucial role in shaping the discourse around emerging technologies. Additionally, her involvement as an External Expert on the Interview Committee for Project Engineer selection at CDAC Bengaluru (2017 – 2019) underscores her commitment to nurturing talent and driving innovation.



Dr. Vanita Agarwal sharing experiences at Nano Electronics Centre , IIT Bombay

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Report On STTP Attended By Faculty

Day 3: 12/06/2024

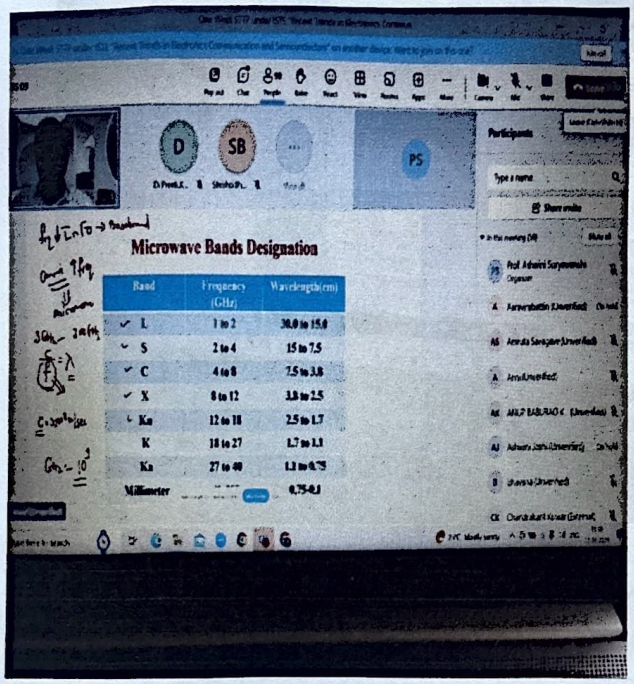
Name of Day 3 SessionCoordinator: Prof. Kishor Jadhav

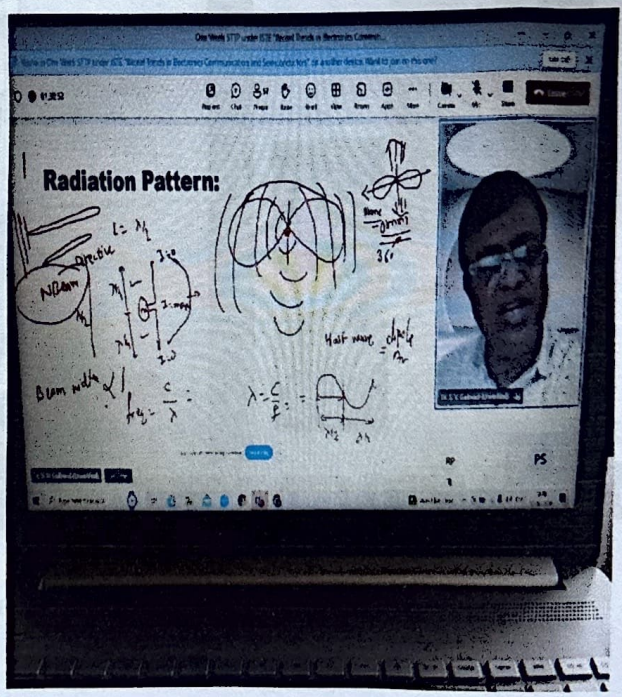
Name of Speaker : Dr. S V Gaikwad for Session

Brief Introduction of Resource Person/Speaker (If Applicable): Dr. S V Gaikwad is working as Associate Professor at PICT, Pune.

Session 1 and Session 2 : Microwave Communication

Dr. S. V.Gaikwad received D.E.R.E. (Diploma) from CWIT, B.E., M.E. (Microwave) and Ph.D. in Electronics and Telecommunication from SPPU (University of Pune). He has 10 years industry experience and 18 years teaching experience. His research area includes design of an Antenna, Microwave techniques in Agriculture, Impact of microwave radiation etc. during research, associated with IIT Powai- campus, Mumbai. His publication are 20+ in International Journals and Conferences. He was invited speaker at International Microwave Power Institute, USA.





Dr. Sandeep V Gaikwad Presenting ISTE STTP Session on Microwave Communication

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Report On STTP Attended By Faculty

Day 4: 13/06/2024

Name of Day 4 SessionCoordinator: Prof. Vaishali Bhimte

Session 1 - CMOS technology (10:00 am – 01:00 pm)

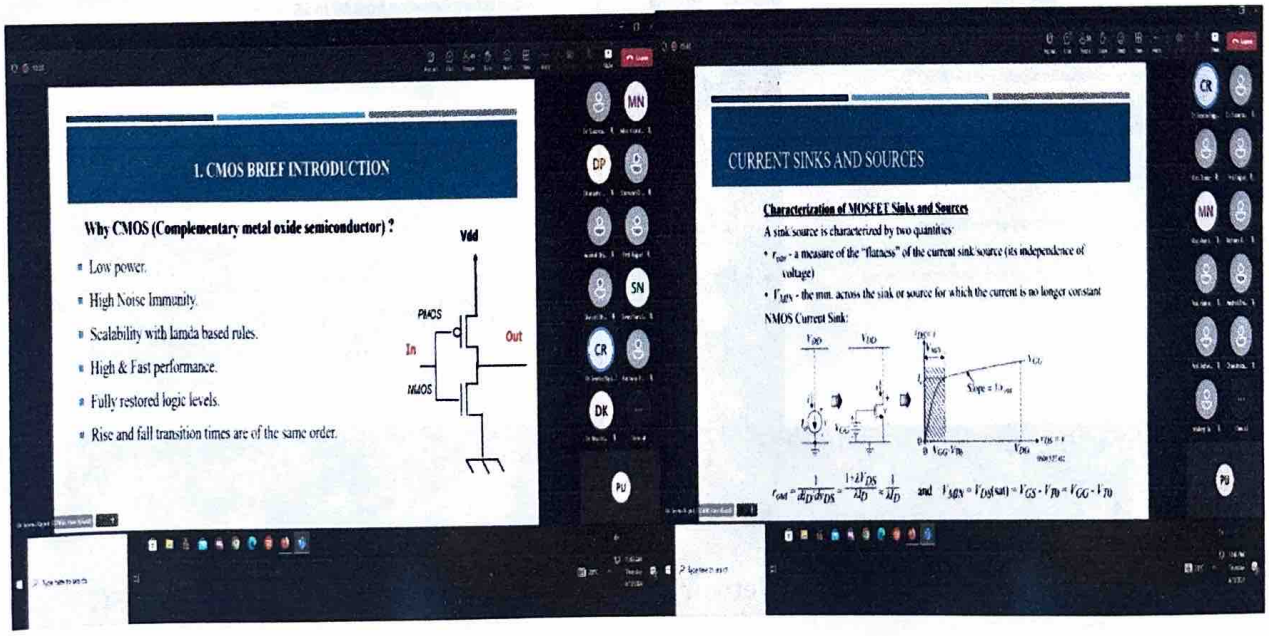
Name of Resource Speakers: Dr. Seema Rajput

Brief Introduction of Speaker:

Dr. Seema Rajput completed PhD. in Electronics & Telecommunications in 2016 from Nagpur University.She is presently working as an Associate Professor at CCOEW, Pune. She is having total Working Experience of more than 23 Years. She has published several papers in reputed international and national journals. She has received Grant of Rs. 86 lakh by Govt. of India under Chip to startup program as co-chief-investigator. She is Head faculty co-ordinator of Start up and innovation cell at CCOEW. She is awarded with "Best Teacher Award" at Sinhgad Academy of Engineering, Kondhwa, Pune

Brief Description of Session:

Dr. Seema Rajput mam explain about CMOS brief introduction, CMOS fabrication process, CMOS digital logic circuits, Technology scaling, VLSI Design flow, Cadence simulation, Layout Design Rules, stick diagrams and CMOS analog circuits. She has mainly focused on CMOS fabrication process and CMOS digital designs in detail. She has interacted with participants during the session. Participants have asked many questions during the session.



CMOS Brief Introduction &Current sink and Sources Information

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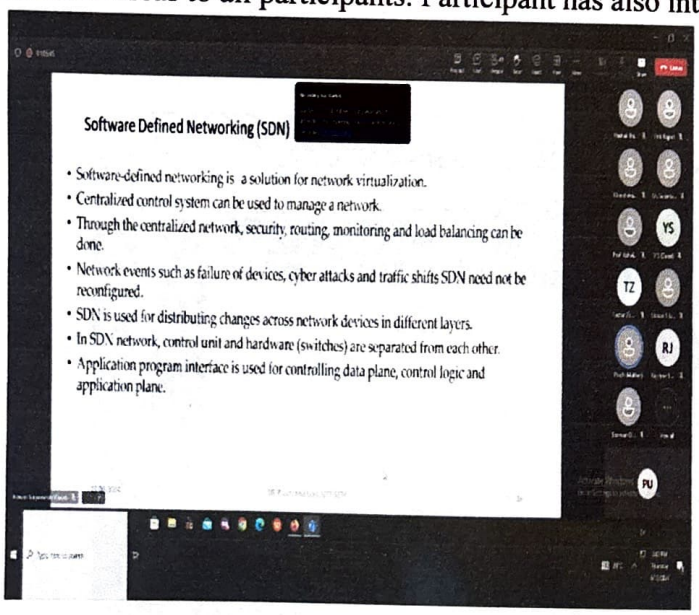
Report On STTP Attended By Faculty

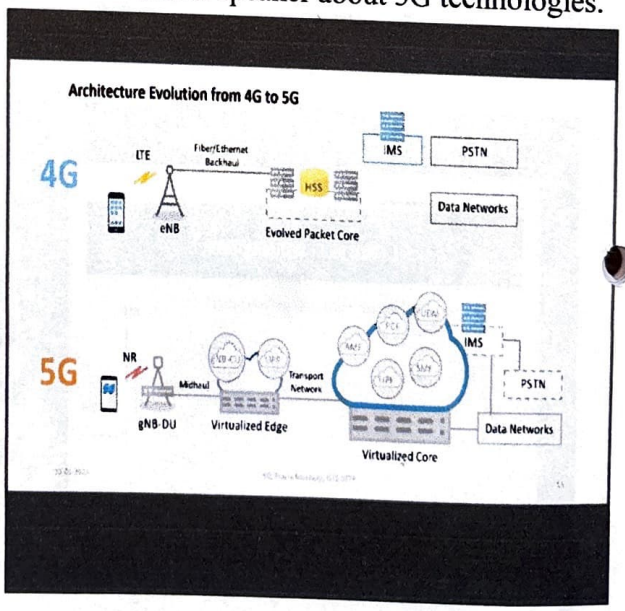
Session 2 - 5G technology (02:00 pm – 05:00 pm)

Name of Resource Speakers: Dr. Prachi Mukherji

Brief Introduction of Speaker: Dr. Prachi Mukherjiis currently professor in Electronics and Telecommunication Department and thedean, of Cummins College of Engineering for Women, Pune. She completed her PhD from SPPU with COEP centre in 2009. She has thirty years of experience in teaching. She is the Chief Investigator of the C2S project grant of approx. one crore, received from MeitY. She has more than 80 publications in referred journals and conferences. She also has a patent. She is a recipient of multiple awards including the prestigious National Level Smt. Triveni Devi Gupta Memorial Award by IETE. She is a Senior Member IEEE and Fellow, IETE. Her areas of research are Signal Processing, Communication and Machine Learning. She is on CDC committee of Colleges, Member of E&TC BOS of SPPU, and session chair in conference, Speaker in AICTE and ATAL FDPs and reviewer of Journals.

Brief Description of Session: Dr. Prachi Mukherji conducted session on 5G technology. She has focused on why 5G,three pillars of 5G,5G Network,5 G Core features, SDN and Future scope release. She has covered network evolution from 4G to 5G.She also covered 5G network spectrum. She has also suggested SDN research areas to all participants. Participant has also interacted with session speaker about 5G technologies.





Introduction to Software Defined Networking&Architecture evolution from 4G to 5G

Anantrao Pawar College of Engineering & Research Pune-9 Pune

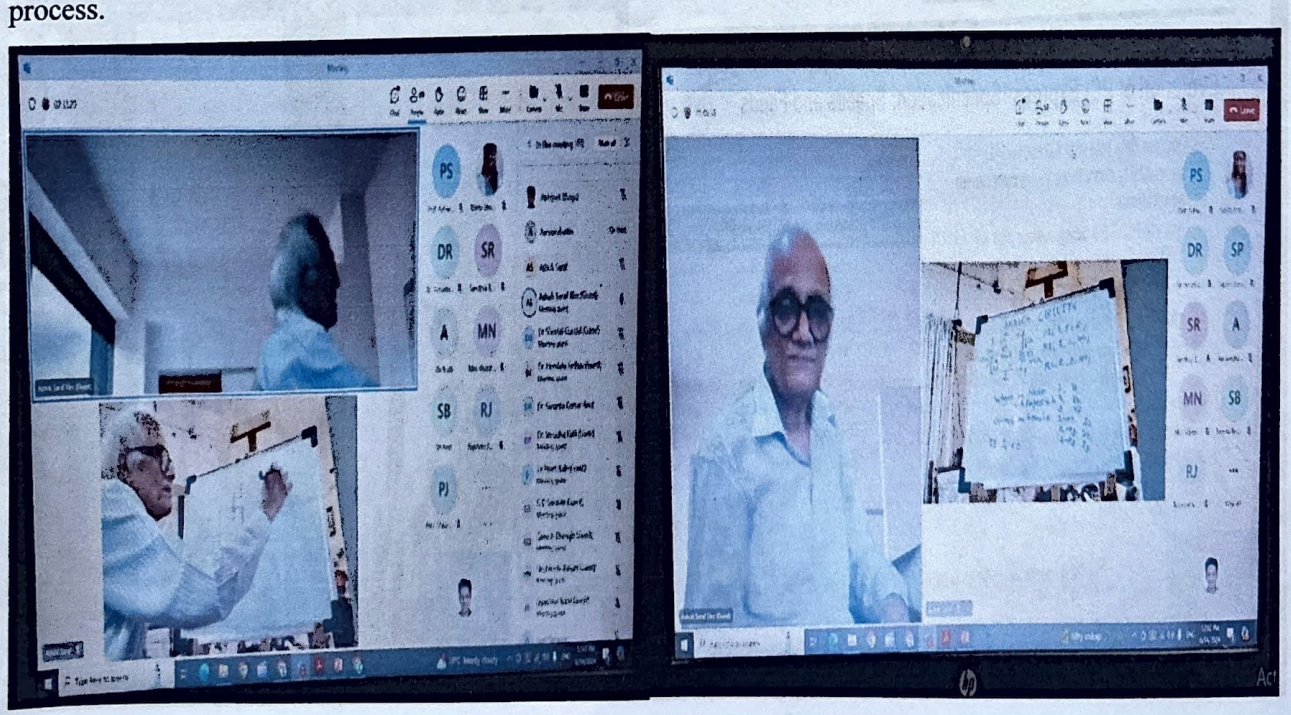
	AkhilBharatiya Maratha ShikshanParishad's **Anantrao Pawar College of Engineering & Research**	
	Record No.: ACA/D/021B **DoI: 02/01/2023** **Revision: 00**	

Report On STTP Attended By Faculty

Day 5: 14/06/2024

Name of Day 5 SessionCoordinator: Prof. Nikita Bhagat
Session 1 - Design of CMOS Analog Circuit (10:00 am – 01:00 pm)
Name of resource Speaker: Mr. Ashok Saraf
Brief Introduction of Speaker:
Mr. Ashok Saraf received B. Tech Electrical Engineering in 1973, IIT Bombay, ME in Digital Communication, Philips International Institute, Eindhoven in 1975. He is Innovation Club Member at APCOER, Pune. He has Total 45 years of experience in various fields. He worked as a research leader for India Center of world's largest research organization "Battle Memorial Institute", Ohio Columbus USA. He has been Technical Advisor for Sakal Paper, Kirloskar Pneumatics, Mahindra and Mahindra, Telco, BHEL, Accurate Engineering, Infosys, KPIT Cummins. He is Technical Director at "Syslab Automation Pvt. Ltd.", Pune.

Brief Description of Session:
Mr. Ashok Saraf explained the chosen CMOS analog circuit topology (e.g., Digital Gates, operational amplifier, filters etc.) as well as gave brief about design Requirements, Constraints and considerations during the design process.



Mr. Ashok Saraf Presenting ISTE STTP Session Design of CMOS Analog Circuit

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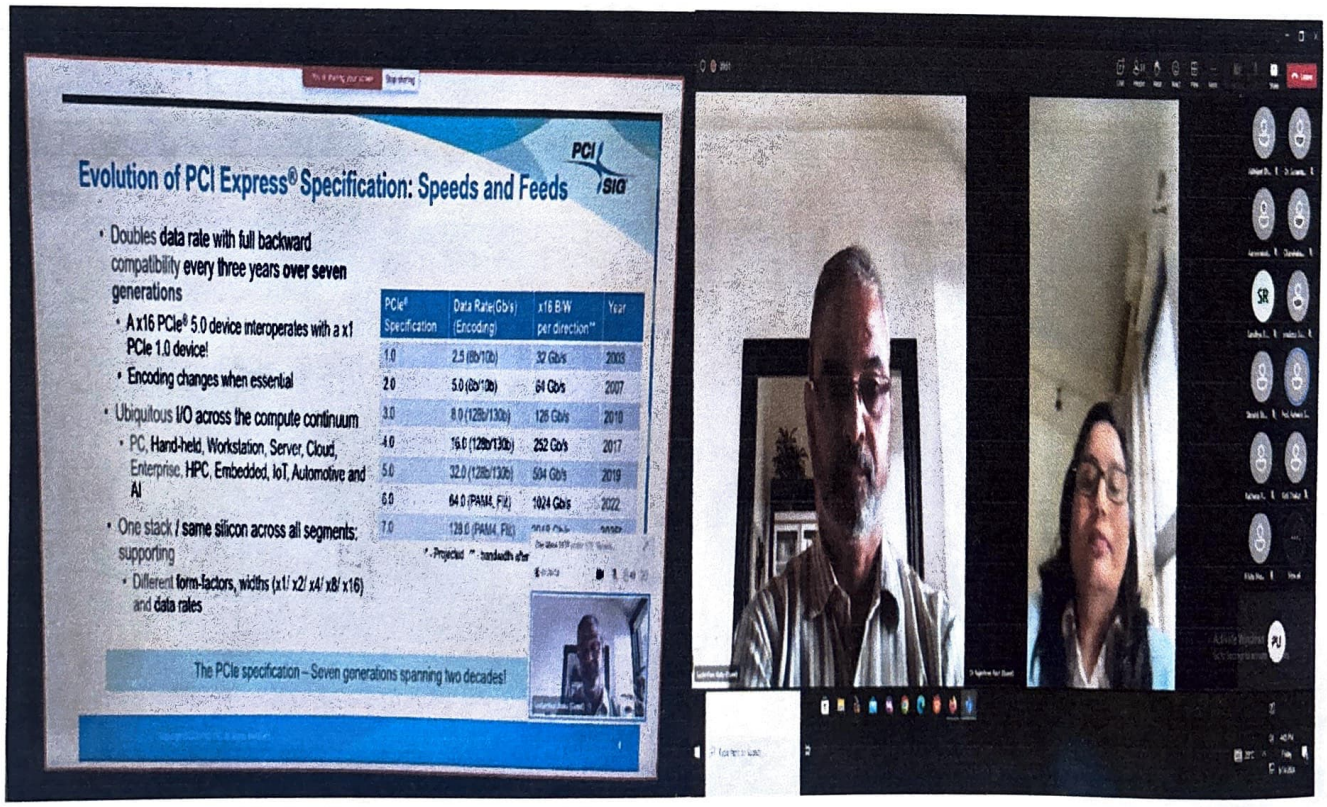
Report On STTP Attended By Faculty

Session 2- IP Development Platform based on FPGA Technology-Experience Sharing (02:00 pm – 05:00 pm)
Name of resource Person/ Speaker (If Applicable): Mr. Sudarshan Natu
Brief Introduction of Speaker:
Mr. Sudarshan Natu received BE from COEP, M.Tech in Communication from IIT Bombay in 1982. He is Innovation Club Member at APCOER, Pune. He has Total 38 years of industry experience, currently working as a Mentor and consultant to startups and product based companies. He has expertise in VLSI Design, FPGA Design, IP Design. He has awarded "Yashokirti Puraskar" for contribution in IT field. He has awarded by Government of Maharashtra for "Best Exporting Company" in 1998.

Brief Description of Session:
Mr. Sudarshan Natu explained the purpose of developing the IP and its intended use. He discussed the importance of FPGA-based IP development in modern digital design. Also Sudarshan Natu shared their experience with us related to IP Development Platform based on FPGA Technology was not only informative but also highly engaging.



Mr. Sudarshan Natu Presenting ISTE STTP Session IP Development Platform based on FPGA Technology-Experience Sharing

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Report On STTP Attended By Faculty

Valedictory Session

Date: 12/07/2024

Prof. Ashwini A Suryawanshi
Event Coordinator

Dr. Amar B. Deshmukh
Head of Department

Dr. Sunil B. Thakare
Principal

Anantrao Pawar College of Engineering & Research
Pune
Pune-9

Akhil Bhartiya Maratha Shikshan Parishad's

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Internal Correspondence For Department

Date- 12/06/2024

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STTP Co-ordinator