



ABMSP's
Anantrao Pawar College of
Engineering & Research, Parvati,
Pune-09



In Association With

Vidyanjali- A Higher Education Volunteer Programme,
Ministry of Education, Government of India.

Organizing
18th Expert Session
on



“Overview of VLSI Design”

Date : 16/08/2024

Time : 11:00 AM – 01:00 PM

Mode of Conduction &

Platform : Online, Google Meet

Meeting Link :

meet.google.com/tio-dhss-dcg

Vidyanjali- Institute Nodal Officer (INO) :
Asst.Prof. Krantikumar V. Mhetre

Subject Teacher :
Asst. Prof. Vaishali V. Bhimte



Mrs. R. Krishnaveni
Assistant Professor,
ECE Engineering,
MAM College of
Engineering,
Tiruchirappalli,
TamilNadu, India.

Dr. Amar B. Deshmukh
HoD E&TC, APCOER

Dr. Sunil B. Thakare
Principal, APCOER

Mrs. Pramila Gaikwad
General Secretary,
ABMSP

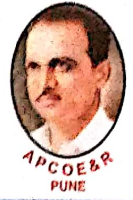


AKHIL BHARATIYA MARATHA SHIKSHAN PARISHAD'S
ANANTRAO PAWAR COLLEGE OF ENGINEERING & RESEARCH

Sr. No. 103, Parvati, Pune - 411 009.

Tel.: 020-24218901/8959/3929

Web.: <http://www.abmspcoerpune.org> • Email : office@abmspcoerpune.org



Approved by AICTE & Govt. of Maharashtra, Affiliated to Savitribai Phule Pune University

DTE CODE :- EN 6794, AISHE CODE :- C-41484

Savitribai Phule Pune University id : CEGP019670

Accredited By NAAC With 'A' Grade



Ref.: APCOER/OFFICE/ **384** /2024 -25

Date: 12/08/2024

To,
Mrs. R. KRISHNAVENI
Assistant Professor,
Electronics and Communication Engineering Department,
M.A.M. College of Engineering,
Trichy - Chennai Trunk Road, Siruganur,
Tiruchirappalli - 621 105, Tamil Nadu, India.

Subject: To deliver an expert session at APCOER through Vidyanjali scheme as a Volunteer.

Respected Madam,

With reference to the request created from our end on Vidyanjali portal for conducting a session on "Overview of VLSI Design" for under-graduate students of Electronics & Telecommunication Engineering, we are pleased to receive your support to accept the request. It gives us an immense pleasure to invite you for delivering the expert session through online mode. The details of the session are given below:

Session Date: 16/08/2024

Time: 10:00 AM – 12:00 PM

Mode & Platform: Online- Google Meet

Meeting Link: meet.google.com/tio-dhss-dcg



Prof. Vaishali V. Bhimte
Subject Teacher

Prof. Krantikumar V. Mhetre
Vidyanjali:
Institute Nodal Officer

Dr. Amar B. Deshmukh
Head-
E&TC Engineering

Dr. Sunil B. Thakare
Principal



	Akhil Bharatiya Maratha Shikshan Parishad's Anantrao Pawar College of Engineering & Research		
	Record No.: ACA/D/021 Revision: 00	DoI: 02/01/2023	
EVENT REPORT			

Name of Event: Expert session on “Overview of VLSI Design” under Vidyanjali Initiative.

Venue of Event: E&TC Engineering Department, Online (Google Meet).

Date of Event: 16/08/2024.

Time of event: 11:00 AM to 1:00 PM

Name of Event Coordinators:

Asst. Prof. Krantikumar V. Mhetre (Vidyanjali-Institute Nodal Officer)

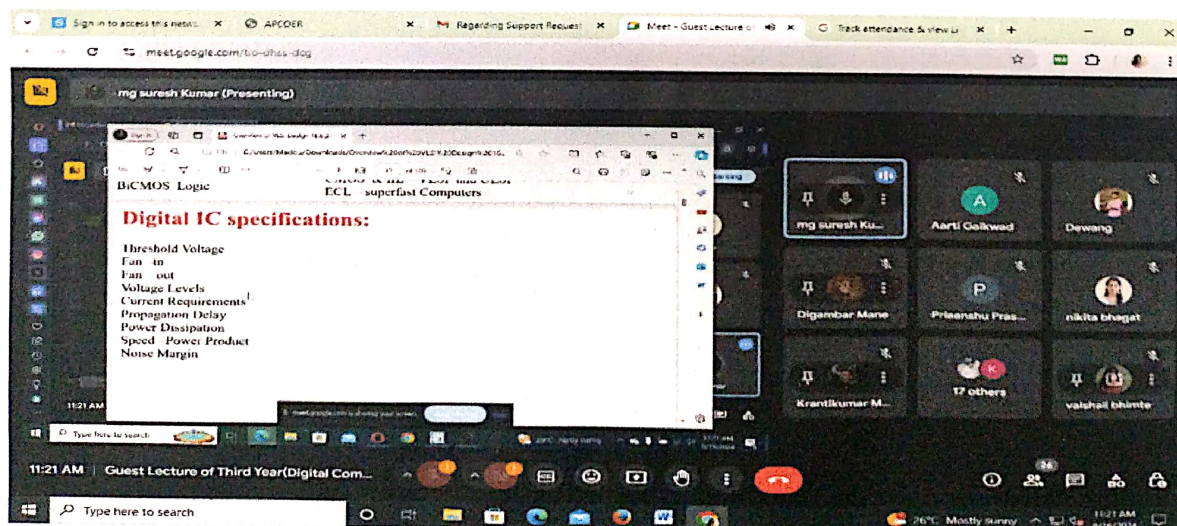
Asst. Prof. Vaishali V. Bhimte (Subject Teacher)

Target Audience with count: 41 students

Brief Description of Session:



The Session started with the brief introduction of Prof. R. KRISHNAVENI madam, as the expert person for the session by Asst. Prof. Krantikumar V. Mhetre. The Session was arranged for students of the E&TC Engineering Department. Mrs. R. KRISHNAVENI Assistant Professor, Electronics and Communication Engineering Department, M.A.M. College of Engineering, Trichy - Chennai Trunk Road, Siruganur, Tiruchirappalli - 621 105, Tamil Nadu, India has started the session. Madam explained about the basic of VLSI Design and its applications. Madam explained in depth about logic design and physical design by sharing the practical real-life examples related to Electronics Engineering perspective. Madam also explained about the various tools available in the market for VLSI Design and applications. Finally, Madam has addressed the questions asked by the students at the end of the session. Vote of thanks was given by Asst. Prof. Krantikumar V. Mhetre.

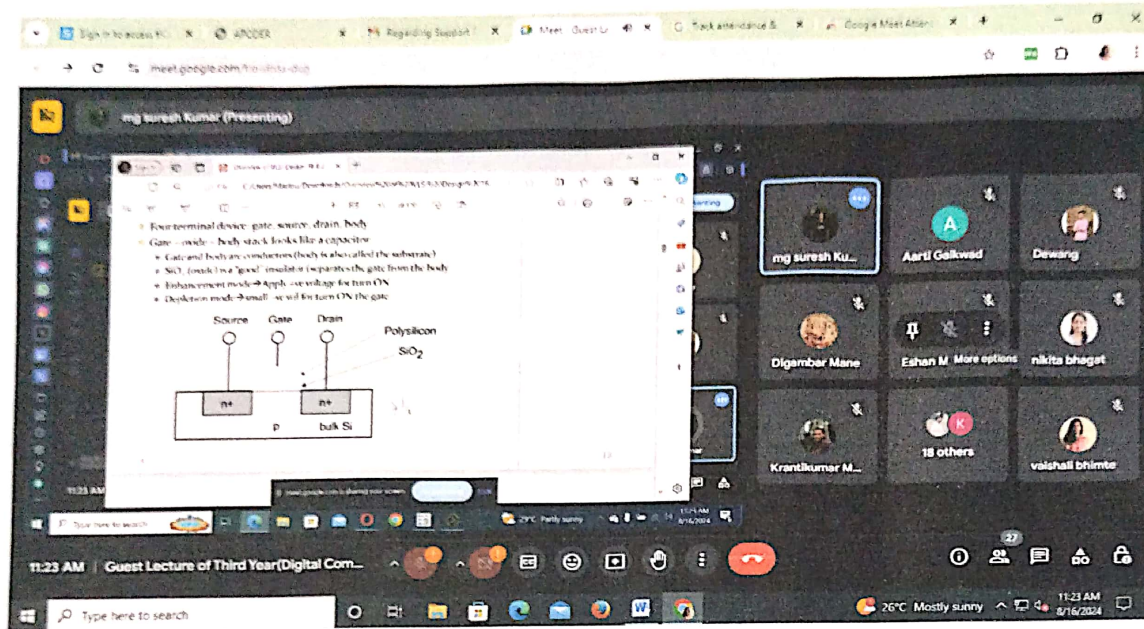
Photographs:



Prof. R. KRISHNAVENI explaining the Digital IC Specification

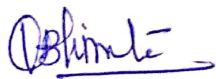



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	Record No.: ACA/D/021 Revision: 00	DoI: 02/01/2023	
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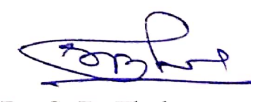
Prof. R. KRISHNAVENI explaining the construction of FET

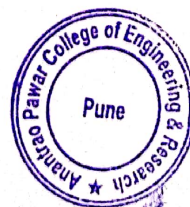
Date: 16/08/2024


Prof. V. V. Bhimte
 Subject Teacher


Prof. Krantikumar V. Mhetre
 Vidyanjali: Institute Nodal
 Officer (INO)


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 Principal

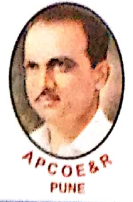




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Record No.: ACA/D/008D	Revision: 00	DoI: 02/01/2023
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Letter of Thanks

To,

Mrs. R. KRISHNAVENI

Assistant Professor,

Electronics and Communication Engineering Department,

M.A.M. College of Engineering,

Trichy - Chennai Trunk Road, Siruganur,

Tiruchirappalli - 621 105, Tamil Nadu, India.

Respected Madam,

Thank you very much for accepting and delivering the support by you for the expert session at ABMSP's Anantrao Pawar College of Engineering & Research, Parvati, Pune. We would like to express our gratitude towards you for coordinating and sharing helpful insights on the subject “**Overview of VLSI Design**” for our students on 16/08/2024 from 11:00 AM to 01:00 PM through online mode under the **Vidyanjali initiative**.

Thank you for extending your support.

Date: 16/08/2024

Prof. Vaishali V. Bhimte
Subject Teacher

Prof. Krantikumar V. Mhetre
Vidyanjali:
Institute Nodal Officer

Dr. Amar B. Deshmukh
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