	Akhil Bharatiya Maratha Shikshan Parishad's Anantrao Pawar College of Engineering & Research, Parvati,Pune	
Record No.: ACA/R/003B	DoI: 02/01/2023	
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SE Electronics Engineering (VLSI Design & Technology)

Academic Year 2024-25 TERM II

W. E. F. : 01/01/2025

Day	Class	9.00 AM to 10.00 AM	10.00AM to 11.00 AM	11.00 AM to 11.15 AM	11.15 AM to 12.15 PM	12.15 AM to 1.15 AM	1.15 PM to 2.00 PM	2. 00 PM to 3.00 PM	3.00 PM to 4.00 PM	4:00 to 5:00 pm
Monday	S.E. (VLSI)	SS SV	PCS GGB	SHORT BREAK	OOP HV	CS YSS	LUNCH BREAK	ESD GGB	S&CS LAB S2 SV OOP LAB S3 GGB VLSI LAB S1 YSS	
Tuesday		PCS GGB	SS SV		CS YSS	OOP HV		ESD GGB	S&CS LAB S3 SV OOP LAB S1 GGB VLSI LAB S2 YSS	
Wednesday		OOP HV	CS YSS		SS SV	CS YSS		SS SV	PCS LAB S3 GGB VIRTUAL LAB S1 VIRTUAL LAB S2	
Thursday		PCS GGB	SS-TUT SV		PCS LAB S2 GGB ESD LAB S3 SV ESD LAB S1 YSS			S&CS LAB S1 SV OOP LAB S2 SV GGB VLSI LAB S3 YSS	MENTOR MENTEE/ LIBRARY	
Friday		PBL LAB S1 YSS PBL LAB S2 SV PBL LAB S3 GGB			PBL LAB S1 YSS PBL LAB S2 SV PBL LAB S3 GGB			PCS LAB S1 GGB ESD LAB S2 YSS VIRTUAL LAB S3	OOP HV	

Subject	Subject In-charge
Signals & Systems	Prof.Snehal Veer
Control Systems	Prof.Yogesh Santwani
Principle of Communciation Systems	Prof.Ganesh Bhadane
Object Oriented Programming	Dr.Hrishikesh Vanjari
Project based Learning	Snehal V,Yogesh S,Ganesh B
Employbility Skill Development	Ganesh B,Snehal V,Yogesh S

Yogesh.. 30.12.24

Prof. Y.S.Santwani
TIME TABLE COORDINATOR

30/12/24

Prof.Snehal Veer
HOD

Dr. S. B. THAKARE
PRINCIPAL